OIPE JC153 FEB 0 1 2001 PATENT & TRADEMARK OFFICE
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FORM PTO-1390 (REV 10-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

ATTORNEY'S DOCKET NUMBER: 2206-3750.1US

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 09/762074

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US99/16995	27 July 1999	30 July 1998

TITLE OF INVENTION: VIDEO CONFERENCE INTERFACE

APPLICANT(S) FOR DO/EO/US: SORENSON VISION, INC.

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. [ ] The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [ ] has been communicated by the International Bureau.
   c. [X] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [ ] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. [ ] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [ ] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

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Items 11 to 16 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [X] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [ ] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. [ ] Other items or information:

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number: EL700256478US

Date of Deposit with USPS: January 29, 2001

Person making Deposit: Jared Turner

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/762074	PCT/US99/16995	2206-3750.1US

17. ☐ The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**		
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 690.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	- 20 =		X **$18.00**	$ 72.00	
Independent claims	- 3 =		X **$80.00**	$ 80.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$270.00**	$	
TOTAL OF ABOVE CALCULATIONS =				$	
☒ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$ 421.00	
SUBTOTAL =				$ 421.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 421.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 40.00	
TOTAL FEES ENCLOSED =				$ 461.00	
				Amount to be refunded:	$
				charged:	$

a. ☒ ~~A check~~ Checks in the amount of $ 461.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-1469. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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REGISTRATION NUMBER
30,549

09/762074
Rec'd PCT/PTO 29 JAN 2001
PCT/US99/16995

VIDEO CONFERENCING INTERFACE

This application claims the benefit of U.S. Provisional Application No. 60/094,646, filed 30 July 1998.

TECHNICAL FIELD

This invention relates to video conferencing systems and, more specifically, to a system which interfaces with one or more of a plurality of video input and one or more of a plurality of output devices.

BACKGROUND

Video conferencing systems are typically designed for use with one particular type of video input device, such as an NTSC camera ("NTSC" means the North American and Japanese analog video standard), a PAL camera ("PAL" means the European analog video standard), a digital camera, or a high speed serial interface camera (*e.g.*, a FireWire or Universal Serial Bus (USB) camera). Such systems are also typically designed for use with one particular output device, such as an NTSC or PAL video monitor, a television set, a Liquid Crystal Display (LCD) screen, or a computer monitor.

Systems having an interface for video conferencing systems that allow the users or manufacturers of such systems to intermingle video input and output devices as they choose, or as a particular video conferencing application dictates, rather than being required are not known. That is, existing systems are believed to require a particular video input device and a particular output device dictated by the video signal formal for the selected video conferencing system.

DISCLOSURE OF INVENTION

A video conferencing interface is part of a standards-based video conferencing system with excellent video and audio quality, high compression, and great flexibility, all at a low cost. The interface includes an Application Specific Integrated Circuit (ASIC) that incorporates a unique blend of computation and data path designs implemented in hardware, as well as processing and control developed for flexibility using a standard processor.

The "hybrid" method of computation and control available in the disclosed system provides an advantage over "single solution" counterparts in which computation and control is implemented in dedicated hardware only. The use of dedicated hardware

only leads to relative inflexibility in bit rate control. The "hybrid" method of computation and control in the disclosed system provides and an advantage over counterparts that use a software-programmed processor only, thereby abandoning the speed advantages of a hardware implementation.

The disclosed system employs hardware to implement or provide for computation and for a data path to provide for high speed data processing at a much faster rate than could be done in a processor-only environment (*i.e.*, software). A standard software based processor allows for flexibility of control so the system can be made adaptable for several different configurations. However, the result is a slower speed because of the software configuration. To attain higher speeds using hardware, a separate hardware configuration would be needed for each variation needed leading to considerable cost and complexities for implementation.

For example, it is often desirable to control the bit rate at which the system interface processes images so an appropriate balance can be struck between the quality of the images processed, on the one hand, and the speed with which images are processed, on the other hand. When rapid motion occurs in the processed images, for example, it is typically desirable to operate at an increased bit rate so that the rapid motion is quickly processed and communicated. However, the high speed processing negatively impacts image quality. When the images to be processed are relatively static from image to image (*e.g.*, frame to frame), it typically is desirable to operate at a reduced bit rate, but with increased image quality. In a hardware-only implementation, such flexibility would have to be hardwired at greater expense, or would simply be unavailable. In a software-only implementation, flexibility is maintained, but at the expense of reduced processing speed. The present invention employs a "hybrid" approach, heretofore unknown, to secure the benefits of a fixed hardware and a fixed software solution.

In the described embodiment of the present invention, the ASIC is the key to implementing this hybrid approach. The ASIC provides a hardwired implementation for computation and data movement while also providing the flexibility inherent in processor-based processing and control.

In addition to the ASIC, the system incorporates a memory to store the video information as it is being compressed and/or displayed. The system also includes

memory and Electrically Erasable Programmable Read Only Memory (EEPROM) for instructions and data storage for the processor, audio input and output, and a MOdulator/DEModulator (MODEM) for telephone/network interface. (The EEPROM and MODEM are actually optional depending on the configuration requirements.)

The ASIC also includes several interfaces that are flexible in their function that allow for several different system configurations with minimal modification or cost impact. These interfaces include the video input, the video output, and the high speed serial interface.

BRIEF DESCRIPTION OF DRAWINGS

In the drawings:

FIG. 1 is a block diagram depiction of a basic ASIC of the prior art suitable for use in processing video signals;

FIG. 2 is a block diagram of the ASIC suitable for use in one form of a video system of the present invention;

FIG. 3 is is a block diagram of the ASIC suitable for use in another form of a video system of the present invention;

FIG. 4 is a block diagram of a high speed serial interface circuit for use with a video system of the present invention;

FIG. 5. is a block diagram of a video input block of an ASIC used with a video system of the present invention;

FIG. 6 is a block diagram of a bus control block of an ASIC used with a video system of the present invention; and

FIG. 7. is a block diagram of a video output block of an ASIC used with a video system of the present invention.

BEST MODES FOR CARRYING OUT THE INVENTION

As shown in Figure 1, a conventional ASIC 10 may be included on a circuit board 12 . The circuit board 12 includes a memory 14 connected to a Memory Control 30 forming a memory module 15 that functions to retain video signals. Memory 14 may be implemented as a dynamic random access memory (DRAM), a static random

access memory (SCRAM), or other suitable memory device architecture known by persons skilled in the art.

The circuit board 12 may also have an optional EEPROM module 16. A separate processor memory module 18 (*e.g.*, SCRAM DRAM, etc.) along with an audio input/output (I/O) module 20 (connected, for example, to a microphone or speaker), and a MODEM and/or Network interface (*e.g.*, LAN or local area network interface) module 22 which together function as a remote video interface circuit 19 may also be included on the circuit board 12.

In one operational configuration, Video-In circuitry 24 receives digital video signals 26 from a single or selected video signal source. "H.263" is a video compression/decompression standard established by the International Telecommunications Union (ITU). H.263 Encode circuitry 34 directs the Memory Control circuitry 30 to forward stored digital video data sent to it from the video memory module 15. The Memory Control circuitry 30 sends the stored video data that it receives out onto and along the memory bus 32. As the H.263 Encode circuitry 34 encodes (*i.e.*, compresses) the stored digital video data, it passes the now encoded digital video data to a MODEM or a Network module 22 for transmission to a remote station (not shown) at which location the digital video data may be decoded and subsequently displayed for viewing by a user. The remote station may include the inventive video conferencing interface described herein, or it may be a conventional video conferencing system interface.

Encoded digital video data is transmitted by and also received from the remote station or another station through the MODEM or the Network 22. The MODEM or the Network 22 transmit and receive data. If a MODEM is used, the signal is modulated and or demodulated and transmitted over an appropriate line such a telephone line or any equivalent thereof. Alternately, it may be transmitted through a network wiring arrangement which is configured to provide video signal transmission.

The data received from the remote location through a MODEM, a network or what ever else may be extant, is transferred through the Processor circuitry 40 to the Bus Control circuitry 36. The Bus Control Circuitry 36 passes the data over the data bus 38 to H.263 Decode circuitry 42 for decoding. After decoding the digital video data, the H.263 Decode circuitry 42 forwards the decoded digital video data to the

Memory Control circuitry 30 over the memory bus 32 for storage in the DRAM 14. Video Out circuitry 44 then directs the Memory Control circuitry 30 to retrieve the stored digital video data from the DRAM 14 for output by the Video Out circuitry 44 in digital form for display by a selected video display device (not shown) connected to receive the video signal from the Video Out Circuitry 44.

Alternatively, serial digital video data, or serial control signals from an attached computer system, can be input or output through high speed serial interface circuitry 46, as will be described in more detail below.

Support circuitry 48 and performs certain "housekeeping" and control functions. The Support circuitry 48 interacts with the EEPROM module 16 via a well-known I^2C bus 50, handling interrupt signals, INT, and reset signals, RST, and programming an array of programmable I/O pins, PIO (not shown).

The EEPROM module 16 may be used to store machine code for the operation of the Processor circuitry 40. At start-up, the machine code can be transferred from the relatively slow EEPROM module 16 to the relatively fast processor memory device 18 for use by the Processor circuitry 40 during normal operations.

The system of the present invention shown in FIG. 2 incorporates a plurality of video input options supplied by video input means 11 the output of which is supplied as the input video signal 26. The input means 11 is here shown to include two or more sources of video signals. The sources illustrated include an Internal Digital Camera 52, an Internal NTSC or PAL video camera 56, an External NTSC or PAL video Camera 58. Input may also be had from an External High Speed Serial Camera 60. Although shown separated from the input means 11, the High Speed Serial Camera 60 can be incorporated into the input means 11 or positioned separately to supply an input signal to the data bus 38.

An "internal" camera 52 is a camera in which the lens and interface control are mounted inside the system enclosure, while an "external" camera interfaces through a connector which may be the video decoder 54.

More specifically, as shown in Figure 2, the digital video signals 26 can be generated by the internal digital camera 52, or by the Video Decoder module 54 converting analog NTSC or PAL signals from the internal NTSC or PAL camera 56 or the external NTSC or PAL camera 58 to the digital video signals 26. Alternatively, or

in addition, a digital camera 60 having a high speed serial output, such as a FireWire or USB port, can output serial digital video signals to the high speed serial interface 46 for further processing and transmission to the data bus 38.

The ASIC 10 of FIG. 2 is configured to have a memory means 15 that includes the DRAM 14 and the memory control 30. Memory control circuitry 30 transfers the digital video signals 26 from a memory bus 32 to the DRAM 14 for storage and also to the H.263 encode module 34 for compression prior to processing by the video processing means 35. The video processing means 35 includes the Processor 40 as well as the support circuit 48 and the bus control 36. It also includes the processor Memory 18 and the EEPROM 16 if provided.

The video processing means 35 and more specifically the Processor circuitry 40 directs the encoded digital video data to the remote interface circuit 19. The remote interface circuit 19 is any suitable circuit to transmit and receive video conferencing signals to and from a remote source. That is, the remote interface circuit 19 is configured to receive video signals and preferably voice signals from a remote source to effect what may be referred to as video conferencing. The outgoing video signals as well as audio signals are sent to a remote location which ideally is returning similar video signals and audio signals for processing by the ASIC and for presentation as a video signal on a selected video display or output device. The remote interface means 19 is here illustrated to include the MODEM 22 and Audio circuit 20.

The ASIC 10 of FIG. 2 has all the other processing circuitry of FIG. 1 as shown in FIG. 2 while at the same time differing significantly in that a plurality of video input arrangements can be accepted from the video input means 11 using a combination of software and hardware to facilitate speed in processing and flexibility.

The system of the present invention in another embodiment depicted in FIG. 3 may also integrate one of several video output options, including NTSC/PAL 68, a Video Modulator 62, LCD 72, RGB 71, and a remote device connected by conductors 73 through the High Speed Serial Interface 46.

More specifically, as shown in Figure 3, the digital video output of the Video Out circuitry 44 can be provided to video output means 43 which is here shown to include a Video Modulator module 62 to convert the digital video output from the video out circuitry 44 to a modulated analog signal 64. The analog signal is then

multiplexed by a Cable Multiplexer module 66 for output as a TV channel (*e.g.*, channel "3") to a monitor 68. Alternatively, the digital video output of the Video Out circuitry 44 can be converted by a Video Encoder module 70 to an NTSC or PAL analog format suitable for input to a dedicated port on the monitor 68, or can be converted into an LCD format signal for an LCD screen 72. In still another alternative, the Video Encoder module 70 can convert the digital video output from the Video Out circuitry 44 to an RGB signal 71 suitable for direct application to a computer monitor (not shown).

The system of the present invention can be configured or modified through the specific use of the High Speed Serial Interface 46 connected to separate video 47 not illustrated in FIG. 3. The video means 47 (FIG. 4), can be used for video input, and/or video output. Additionally, it can be used to connect the system as a peripheral or remote device to another controller. This controller could be, for example, a cable box, a set top box, a personal computer, or any number of general purpose or task specific controller devices. Likewise, this also allows the system to easily be integrated directly into a stand-alone teleconferencing device or video phone.

More specifically, as shown in Figure 4, the depicted ASIC 10 has a High Speed Serial Interface circuit 46 (*e.g.*, a FireWire or USB port) which outputs serial digital video data 71 to video means 47. The video means 47 may include a controller with modem 74, which then interfaces with the telephone system 76 or a separate monitor such as monitor 68.

As shown in Figure 5, the Video-In circuitry 24 includes Input Configuration circuitry 78 that receives digital video signals 26, as well as serial digital video data from the data bus 38. Control register circuitry 80 set by the Bus Control circuitry 36 (*see* Figure 2) causes the Input Configuration circuitry 78 to select and output either the signals 26 or the data from the data bus 38 in a 4:2:2 YUV format. Pixel Decimation circuitry 82 then reduces the "color" component of the output signal, thereby reducing the data density of the signal, by outputting the signal in a 4:1:1 YUV format. Then, a First-In-First-Out (FIFO) buffer 84 holds the output signal before transferring it to the memory means 15 via memory bus 32.

As shown in Figure 6, the Bus Control circuitry 36 includes Bone Interface circuitry 86 for receiving data from the data bus 38 (otherwise known as the

"backbone") and Processor Interface circuitry 88 which communicates with the Processor circuitry 40 (*see* Figure 4). Arbitration and Control circuitry 90 selects which Interface circuitry 86 and 88 will be active at any one time, and Host Interface circuitry 92 communicates data internally to and from the selected Interface circuitry 86 or 88. Data from the Host Interface circuitry 92 proceeds to Data Interface Control circuitry 94, while register information proceeds to Register Interface Control circuitry 96. Both of the circuitry 94 and 96 communicate with Third Party Module circuitry 98, such as FireWire or USB serial-to-parallel circuitry.

As shown in Figure 7, the Video Out circuitry 44 includes Memory Control/Sequencer circuitry 100 that directs the Memory Control circuitry 30 (*see* Figure 1) to provide it with digital video data from the Video Memory module 14 (*see* Figure 1) in the proper sequence. Line Store circuitry 102 then acts as a buffer for storing the video data until two video lines of data are stored. Interpolator circuitry 104 then reverses the actions of the Pixel Decimation circuitry 82 (*see* Figure 5) by interpolating between each two lines of video data it receives to generate a 4:2:2 YUV signal. A storage FIFO buffer 106 then stores the interpolated video data, and Control Registers circuitry 108 controlled by the Bus Control circuitry 36 (*see* Figure 1) then causes Encoder Control circuitry 110 to output the stored video data, or not, as the situation may dictate. At the same time, the stored video data is provided on the data bus 38 to the Bus Control circuitry 36 (Figure 1) for use by the High Speed Serial Interface circuitry 46 (*see* Figure 1).

The systems of FIGS. 2 or 3 can be easily and inexpensively configured as several different devices including, but not limited to: a PC peripheral for camera or video conferencing; a cable box peripheral for camera or video conferencing; and a remote camera for surveillance systems. In addition, the system that includes the circuit of FIGS. 2 or 3 can be integrated into or tightly coupled with other hardware to create other devices including, but not limited to, a set top box video conferencing system; a cable box video conferencing system; and a video phone.

It should be understood, of course, that the systems depicted in Figures 2-7 may be a transmitting or receiving station, or, more likely in most video conferencing systems, both.

The embodiments herein illustrated and described are not intended to limit the scope of the invention as defined in the following claims.

CLAIMS

What is claimed is:

1. A video conferencing circuit for use with a plurality of video input devices and a video output device, said video conferencing circuit comprising:

video input means for providing input video signals from one of a plurality of video signal generating devices;

a remote interface circuit;

a video output device; and

an application specific integrated circuit (ASIC) connected to said video input means, to said video output device and to said remote interface circuit, said ASIC having:

a video-in circuit connected to said video input means to receive a video input signal from one of said plurality of video signal generating devices,

a memory circuit connected to said video-in circuit to receive said video input signal, said memory circuit being configured to retain and transmit said video input signal as stored data,

data compression means connected to said memory circuit to receive said stored data and to compress said stored data through an encoding process to form outgoing compressed data,

video processing means connected to receive said outgoing compressed data and connected to said remote interface circuit to transmit said outgoing compressed data and to receive incoming compressed data from a remote station, said video processing means also being connected to said video-in circuit, said memory circuit, said video decompression means, said video receiving means, and to said video image out means to control the flow of video signals thereinbetween,

video decompression means connected to said video processing means to receive said incoming compressed data and configured to decompress and to transmit said incoming compressed data to said memory circuit, said memory circuit being configured to convert said incoming compressed data to incoming stored data, and

video image out means connected to receive incoming stored data from said memory circuit and to transmit said incoming stored data as a video image signal to a video display device.

2. The video conferencing circuit of claim 1 wherein said remote interface circuit includes a modem.

3. The video conferencing circuit of claim 1 wherein said memory circuit includes a memory structure and a memory control circuit to convert video input signals to stored data and to convert said incoming compressed data to incoming stored data.

4. The video conferencing circuit of claim 3 wherein said memory structure is a DRAM configured to receive and store said stored data and said incoming stored data.

5. The video conferencing circuit of claim 1 wherein said video input means includes a video decoder circuit to receive selected video signals and convert said selected video signals to an input video signal.

6. The video conferencing circuit of claim 5 wherein said video-in circuit includes an input configuration circuit connected to receive a plurality of video input signals, a control register connected to said video processing means to receive control signals therefrom and to said input configuration circuit to supply input control signals to cause said input configuration circuit to operate to supply one of said plurality of video input signals as said video input signal to said memory circuit.

7. The video conferencing circuit of claim 6 wherein said output of said input configuration circuit is supplied to a decimation circuit which operates to reduce the density of the said output signal and is connected to a buffer to store and transmit an output which is a video

8. The video conferencing circuit of claim 1 further including a data bus interconnected between said video-in circuit, said memory circuit, said encoding circuit, said decoding circuit and said video out circuit for transmitting control signals therebetween, and wherein said video processing means includes a bus control circuit connected to said data bus to supply said control signals thereto.

9. The video conferencing circuit of claim 8 wherein said bus control circuit includes a bone interface circuit connected to said data bus, said bone interface circuit being configured to generate and to supply said control signals to said data bus.

10. The video conferencing circuit of claim 9 wherein said video processing means includes a data processor connected to said remote interface circuit, a processor interface connected to said data processor to supply data thereto and a arbitration and control circuit connected to said processor interface and to said bone interface circuit and configured to select and activate one of the bone interface circuit and the processor interface, and a host interface circuit connected to said arbitration and control circuit, said host interface circuit being configured to supply to and receive data from the processor interface and the bone interface circuit, said arbitration and control circuit also being connected o supply and receive video signals to and from an external device for obtaining and displaying video images.

11. A video conferencing circuit for use with a plurality of video output devices and a video input device, said video conferencing circuit comprising:

video output means for providing output video signals to one of a plurality of video output devices;

a remote interface circuit;

a video input device; and

an application specific integrated circuit (ASIC) connected to said video input device, to said video output means and to said remote interface circuit, said ASIC having:

a video-in circuit connected to said video input device to receive a video input signal from said video input device,

a memory circuit connected to said video-in circuit to receive said video input signal, said memory circuit being configured to retain and transmit said video input signal as stored data,

data compression means connected to said memory circuit to receive said stored data and to compress said stored data through an encoding process to form outgoing compressed data,

video processing means connected to receive said outgoing compressed data and connected to said remote interface circuit to transmit said outgoing compressed data and to receive incoming compressed data from a remote station, said video processing means also being connected to said video-in circuit, said memory circuit, said video decompression means, said video receiving means, and to said video image out means to control the flow of video signals thereinbetween,

video decompression means connected to said video processing means to receive said incoming compressed data and configured to decompress and to transmit said incoming compressed data to said memory circuit, said memory circuit being configured to convert said incoming compressed data to incoming stored data, and

video image out circuit connected to receive incoming stored data from said memory circuit and to transmit said incoming stored data as a video image signal to one of said plurality of video output devices of said video output means.

12. The video conferencing circuit of claim 11 wherein said remote interface circuit includes a modem.

13. The video conferencing circuit of claim 11 wherein said memory circuit includes a memory structure and a memory control circuit to convert video input signals to stored data and to convert said incoming compressed data to incoming stored data.

14. The video conferencing circuit of claim 13 wherein said memory structure is a DRAM configured to receive and store said stored data and said incoming stored data.

15. The video conferencing circuit of claim 11 wherein said video-in circuit includes an input configuration circuit connected to receive said video input signal, a control register connected to said video processing means to receive control signals therefrom and to said input configuration circuit to supply input control signals to cause said input configuration circuit to operate to supply said video input signal to said memory circuit.

16. The video conferencing circuit of claim 15 wherein said output of said input configuration circuit is supplied to a decimation circuit which operates to reduce the density of the said output signal and is connected to a buffer to store and transmit an output which is a video

17. The video conferencing circuit of claim 11 further including a data bus interconnected between said video-in circuit, said memory circuit, said encoding circuit, said decoding circuit and said video out circuit for transmitting control signals therebetween, and wherein said video processing means includes a bus control circuit connected to said data bus to supply said control signals thereto.

18. The video conferencing circuit of claim 17 wherein said bus control circuit includes a bone interface circuit connected to said data bus, said bone interface circuit being configured to generate and to supply said control signals to said data bus.

19. The video conferencing circuit of claim 18 wherein said video processing means includes a data processor connected to said remote interface circuit, a processor interface connected to said data processor to supply data thereto and a arbitration and control circuit connected to said processor interface and to said bone interface circuit and configured to select and activate one of the bone interface circuit and the processor interface, and a host interface circuit connected to said arbitration and

control circuit, said host interface circuit being configured to supply to and receive data from the processor interface and the bone interface circuit, said arbitration and control circuit also being connected o

20. The video conferencing circuit of claim 11 wherein said video image out circuit includes:

a memory control sequencer connected to said memory circuit, said memory control sequencer being configured generate and send to the memory circuit instructions to cause the memory circuit to supply said memory control sequencer with said incoming stored data and said memory control sequencer being configured to supply said incoming stored data as an output,

a line buffer connected to receive said incoming stored data from said memory control sequencer, said line buffer being configured to store a video line of said incoming stored data as first video out signal and another video line of said stored video data as a second video out signal,

an interpolator circuit connected to said line buffer to receive said first video out signal and said second video out signal and to generate an interpolated video signal,

a buffer connected to said interpolator circuit to receive said interpolated video signal therefrom,

a control register connected to said data bus to receive control signals from said video processing control and to said buffer to supply signals to cause said buffer to supply said interpolated video signal , and

an encoder connected to said buffer to receive said interpolated video signal therefrom and to said control register to receive signals to cause said interpolated video signal to be supplied as the video image signal to one of said plurality of video output devices of said video output means.

21. A video conferencing circuit for use with a plurality of video output devices and a video input device, said video conferencing circuit comprising:

video output means for providing output video signals to one of a plurality of video output devices;

a remote interface circuit;

video input means for providing input video signals from one of a plurality of video signal generating devices; and

an application specific integrated circuit (ASIC) connected to said video input means, to said video output means and to said remote interface circuit, said ASIC having:

a video-in circuit connected to said video input means to receive a video input signal from one of said plurality of video signal generating devices,

a memory circuit connected to said video-in circuit to receive said video input signal, said memory circuit being configured to retain and transmit said video input signal as stored data,

data compression means connected to said memory circuit to receive said stored data and to compress said stored data through an encoding process to form outgoing compressed data,

video processing means connected to receive said outgoing compressed data and connected to said remote interface circuit to transmit said outgoing compressed data and to receive incoming compressed data from a remote station, said video processing means also being connected to said video-in circuit, said memory circuit, said video decompression means, said video receiving means, and to said video image out means to control the flow of video signals thereinbetween,

video decompression means connected to said video processing means to receive said incoming compressed data and configured to decompress and to transmit said incoming compressed data to said memory circuit, said memory circuit being configured to convert said incoming compressed data to incoming stored data, and

video image out circuit connected to receive incoming stored data from said memory circuit and to transmit said incoming stored data as a video image signal to one of said plurality of video output devices of said video output means.

22. A video conferencing circuit for use with a plurality of video input devices and a plurality of video output devices, said video conferencing circuit comprising:

video input means for providing an input video signal from one of a plurality of video signal generating devices;

a remote interface circuit;

video output means for providing output video signals to one of a plurality of video output devices; and

an application specific integrated circuit (ASIC) connected to said video input means, to said video output device and to said remote interface circuit, said ASIC having means programmable

to receive said input video signal in a separate video signal formats each from one of a plurality of separate video input devices,

to store the received data in as stored data,

to compress said stored data through an encoding process to create outgoing compressed data,

to output the outgoing compressed data through said remote interface circuit to a remote station,

to receive incoming compressed data from a remote station via said remote interface circuit,

to decompress the incoming compressed data through a decoding process,

to store the decompressed data, and

to output the decompressed data through said video output means for display by one of said plurality of video output devices.

23. The video conferencing circuit of claim 22 wherein said remote interface circuit includes a modem.

24. The video conferencing circuit of claim 23 wherein said video input means includes a video decoder circuit to receive selected video signals and convert them to an input video signal.

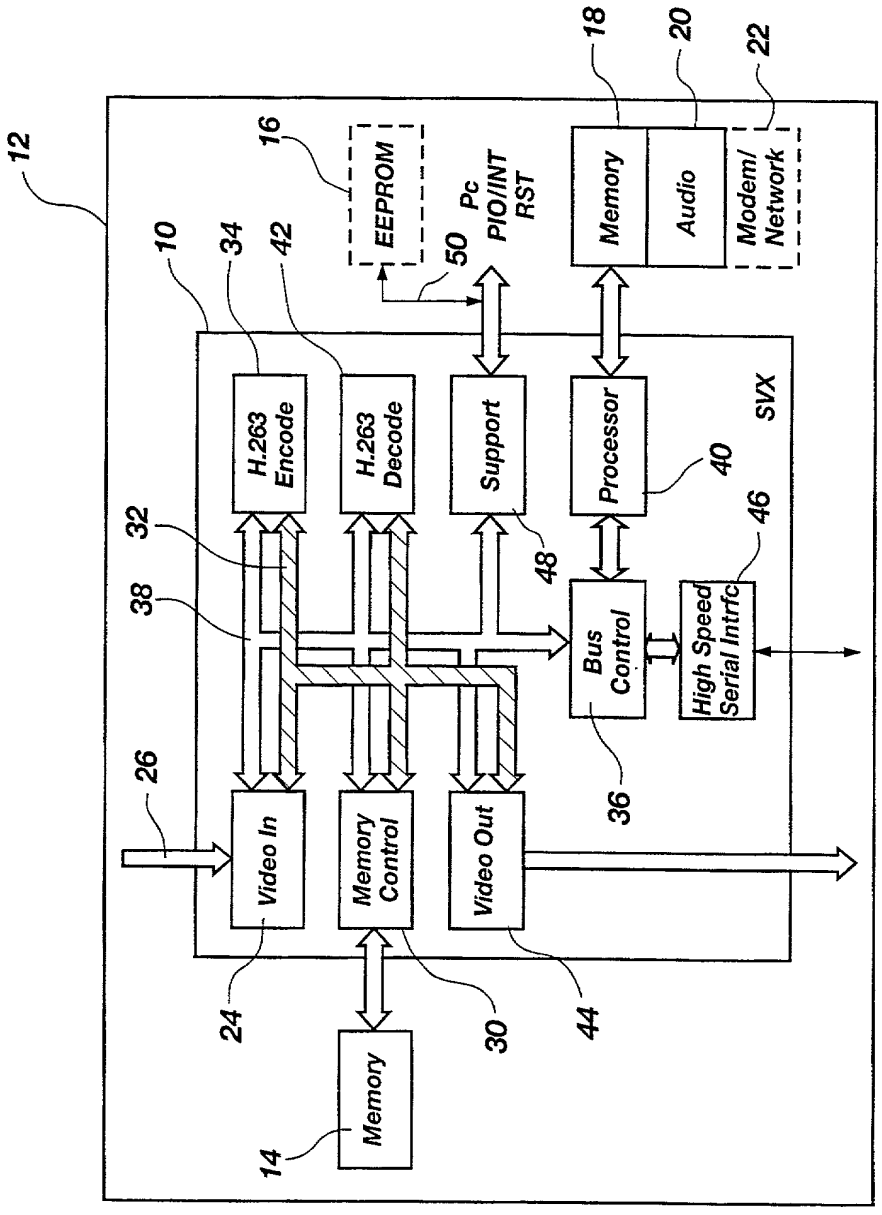
12
16
EEPROM
50
Pc
PIO/INT
RST
18
Memory
20
Audio
22
Modem/
Network
10
34
42
H.263
Encode
H.263
Decode
Support
Processor
40
SVX
32
38
48
46
Bus
Control
High Speed
Serial Intrfc
26
Video In
Memory
Control
Video Out
36
24
30
44
Memory
14

Fig. 1

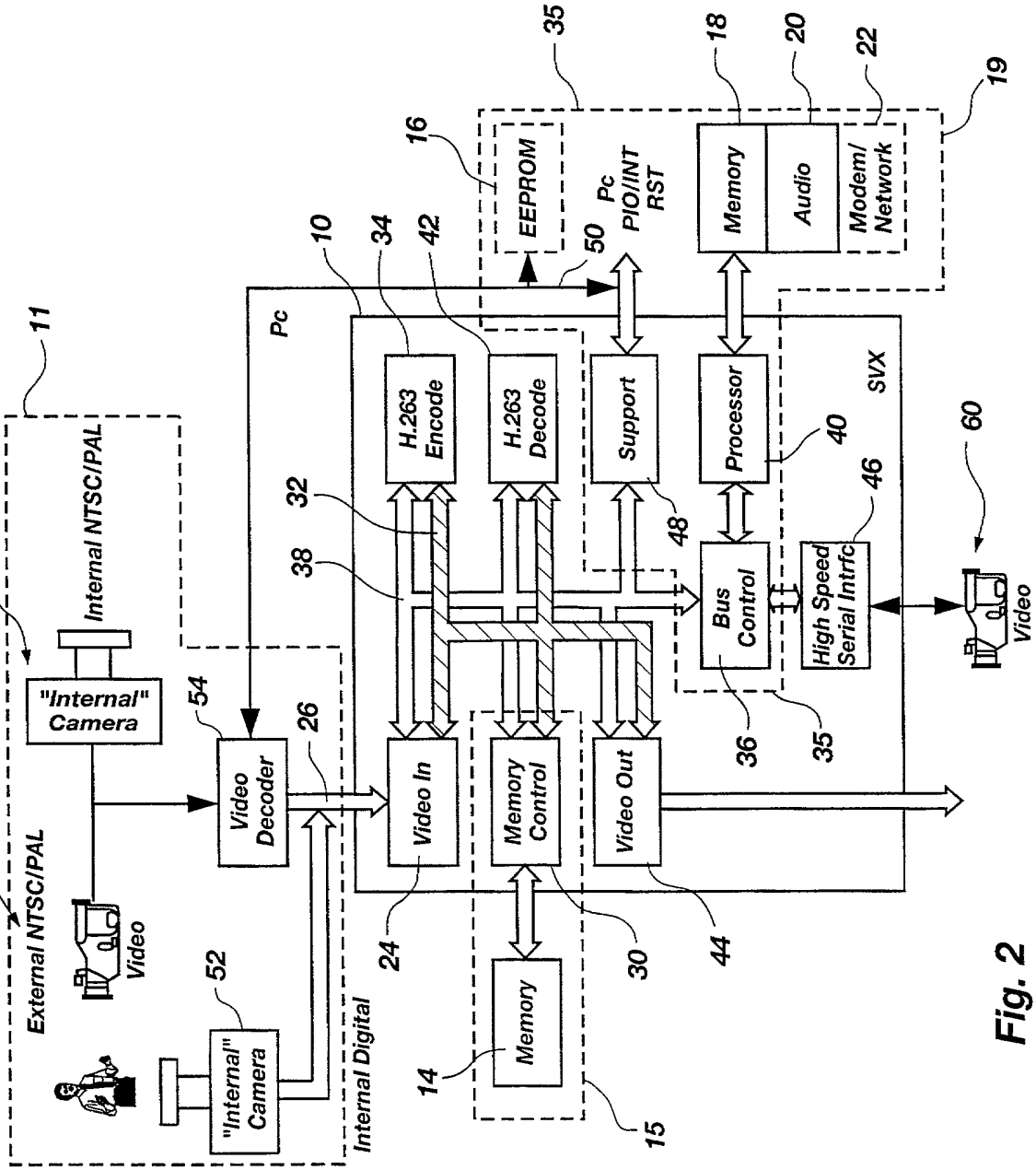
11
Internal NTSC/PAL
56
"Internal" Camera
54
Video Decoder
26
58
External NTSC/PAL
Video
52
"Internal" Camera
Internal Digital
Pc
10
34
42
H.263 Encode
H.263 Decode
32
38
Video In
Memory Control
Video Out
24
30
44
Memory
14
15
35
16
EEPROM
Pc PIO/INT RST
50
Support
48
18
20
22
19
Memory
Audio
Modem/ Network
SVX
Processor
40
Bus Control
36
35
High Speed Serial Intrfc
46
60
Video

Fig. 2

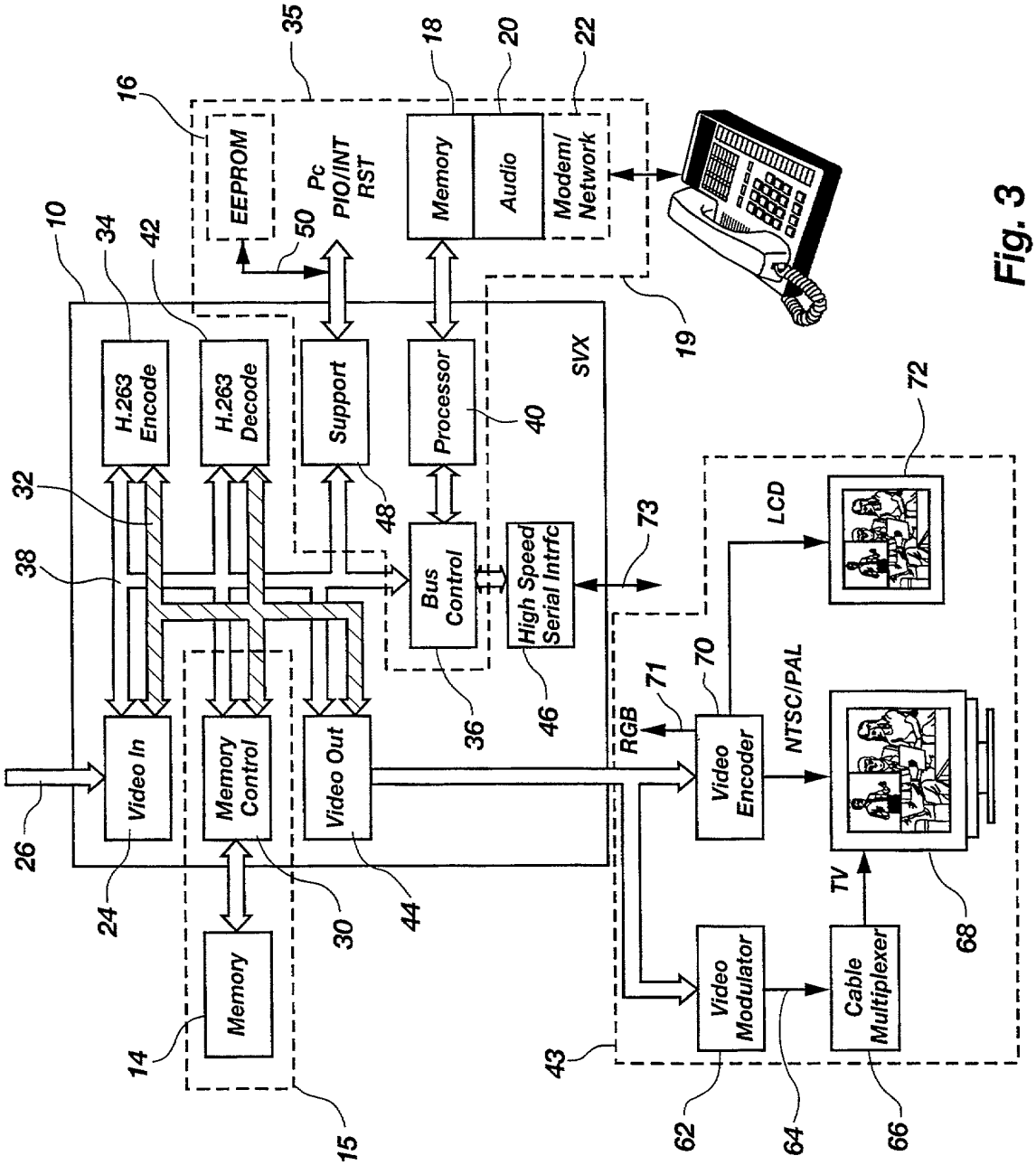
35
18
20
22
16
EEPROM
Pc PIO/INT RST
Memory
Audio
Modem/ Network
10
34
42
50
19
H.263 Encode
H.263 Decode
Support
Processor
40
SVX
72
32
48
73
LCD
38
Bus Control
High Speed Serial Intrfc
71
70
36
46
RGB
NTSC/PAL
Video In
Memory Control
Video Out
Video Encoder
26
24
30
44
TV
68
Memory
Video Modulator
Cable Multiplexer
14
43
62
64
66
15

Fig. 3

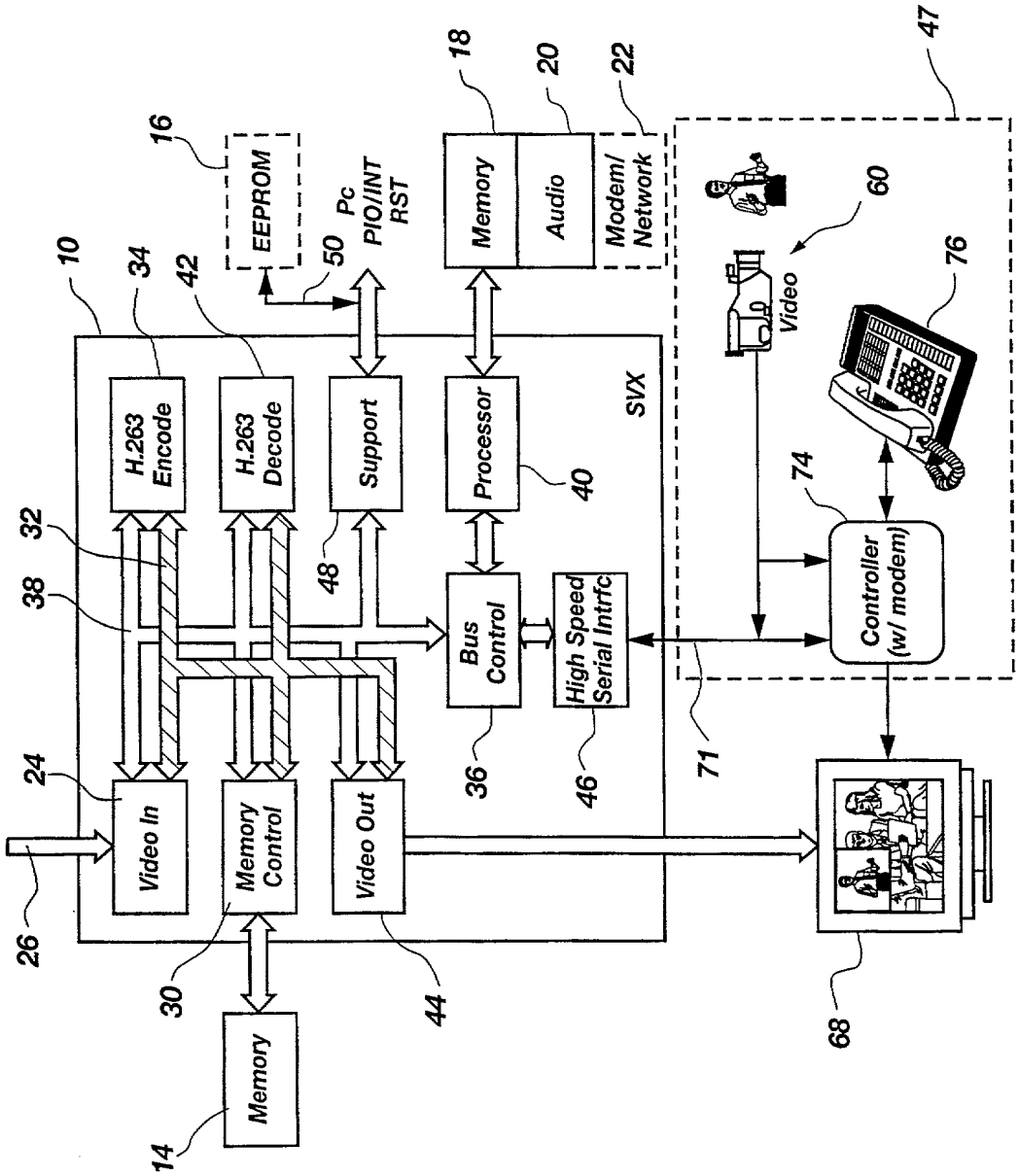
10
16
EEPROM
50
Pc
PIO/INT
RST
18
Memory
20
Audio
22
Modem/
Network
47
60
Video
76
34
42
H.263
Encode
H.263
Decode
Support
Processor
40
SVX
74
32
38
48
Bus
Control
High Speed
Serial Intrfc
Controller
(w/ modem)
24
Video In
Memory
Control
Video Out
36
46
71
26
30
44
68
Memory
14

Fig. 4

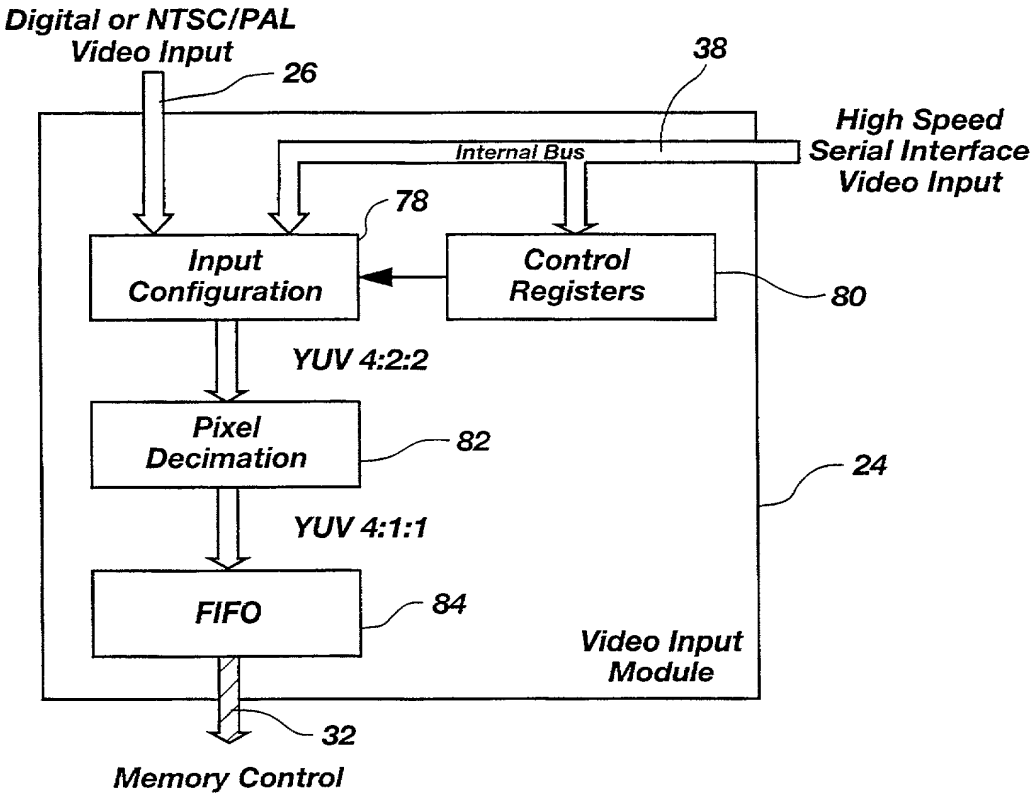
Digital or NTSC/PAL
Video Input
26
38
High Speed
Serial Interface
Video Input
Internal Bus
78
Input
Configuration
Control
Registers
80
YUV 4:2:2
Pixel
Decimation
82
24
YUV 4:1:1
FIFO
84
Video Input
Module
32
Memory Control

Fig. 5

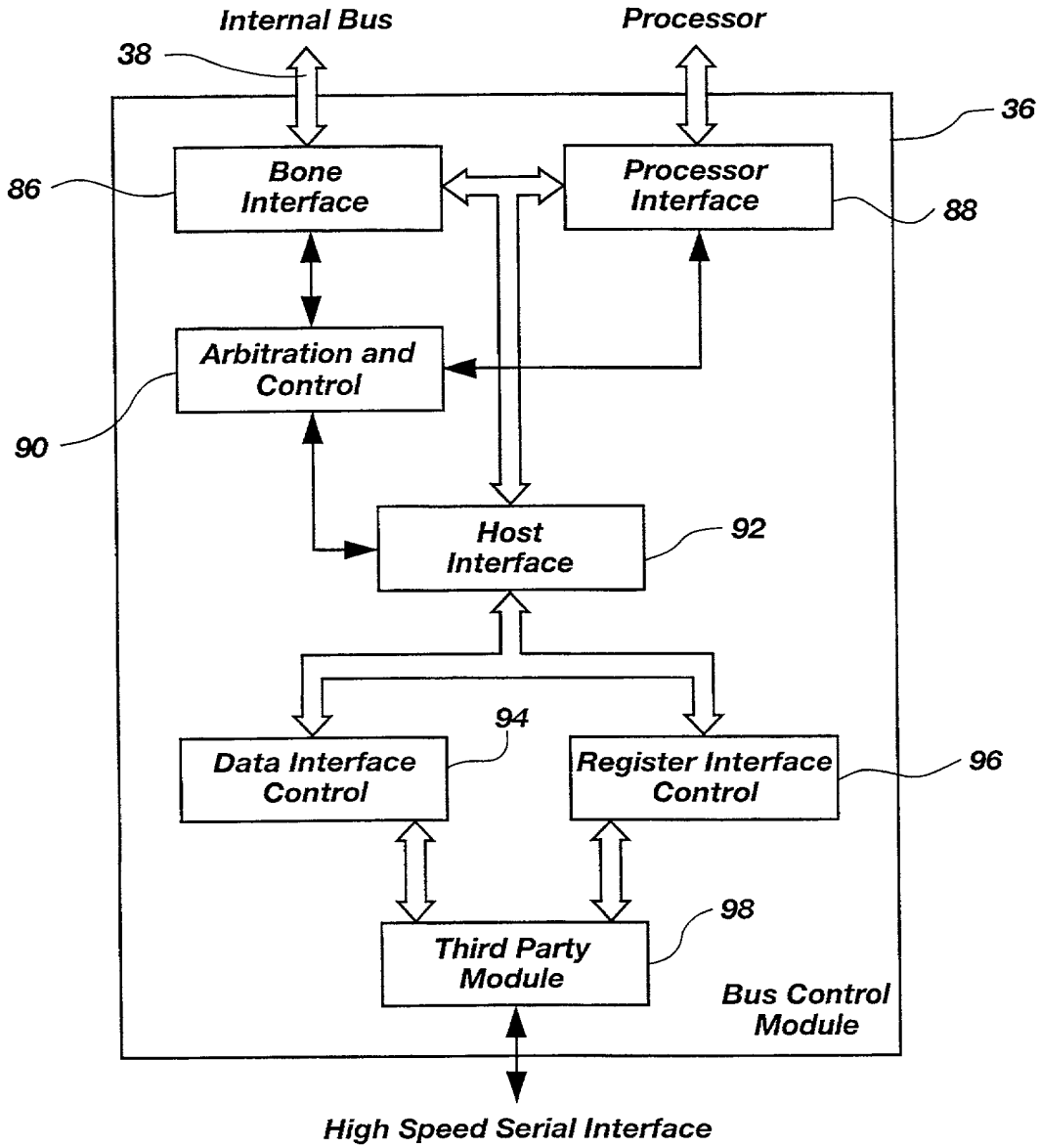
Internal Bus
Processor
38
36
86
Bone Interface
Processor Interface
88
Arbitration and Control
90
Host Interface
92
94
Data Interface Control
Register Interface Control
96
98
Third Party Module
Bus Control Module
High Speed Serial Interface

Fig. 6

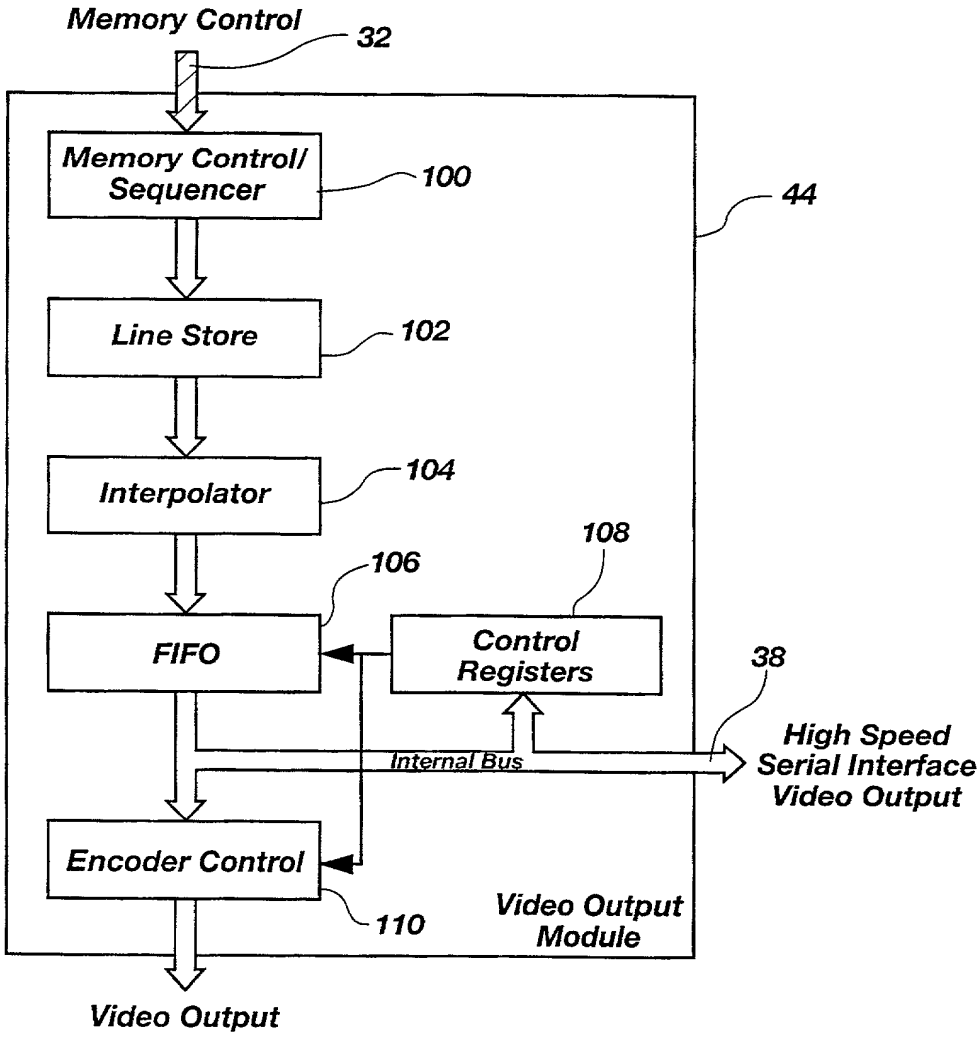
Memory Control
32
Memory Control/ Sequencer
100
44
Line Store
102
Interpolator
104
108
106
FIFO
Control Registers
38
Internal Bus
High Speed Serial Interface Video Output
Encoder Control
110
Video Output Module
Video Output

Fig. 7

Attorney Docket No. 3750.1

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:
My residence, post office address and citizenship are as stated next to my name.
I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled VIDEO CONFERENCING INTERFACE, the specification of which (check one):

☐ is attached hereto.
☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
☒ was filed on 27 July 1999 as PCT international application no. PCT/US99/16995 and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

(number)	(country)	(day/month/year filed)	Priority Claimed Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application:

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

60\094,646 (provisional application no.) — July 30, 1998 (filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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